aluminum. The impedance structure **1080** is relatively insusceptible to ESD events. The impedance structure **1080** can be referred to as a counter current metal bifilar coil in the context of this document.

[0130] Referring to FIG. **11**A, an ESD protection device having a silicon-controlled rectifier (SCR) configuration according to yet another embodiment will be described below. The illustrated protection device **1100** includes a silicon-controlled rectifier (SCR) **1110**, a gate resistor **1112**, a timer **1120**, a first voltage source **1130**, a second voltage source **1140**, a base impedance block **1160**, an emitter impedance block **1170**, and first to fifth nodes N**1**-N**5**.

[0131] The SCR **1110** can have an anode electrically coupled to the first voltage source **1130** via the second node N**2**, a cathode electrically coupled to the emitter impedance block **1170** via the first node N**1**, and a gate electrically coupled to the gate resistor **1112** via the third node N**3**. The cathode and anode of the SCR **1110** can be electrically coupled to first and second nodes, respectively, of an internal circuit to be protected. For example, the first and second nodes can be any two of the nodes **161**, **162**, **163**, **164** of FIG. **1**. For a symmetric SCR device, the anode and cathode are the same, and therefore the polarities of connections to the SCR device do not matter. However, for a non-symmetric SCR device, the SCR device should be correctly connected to voltages references, such as Vcc and Vee. Other details of the SCR **1110** can be as described above in connection with any one or more of FIG. **7**A, **7**B, **8**A-**8**C, **9**A, or **9**B.

[0132] The gate resistor **1112** can have a first end coupled to the third node N**3**, and a second end coupled to a voltage reference, for example, ground. The gate resistor **1112** can have a resistance R**3** of about 1 kΩ to about 30 kΩ for example, 15 kΩ.

[0133] The timer **1120** serves to delay the switching on of the base impedance block **1160**. The timer **1120** can be an RC timer, and can include a timer capacitor **1131**, and a timer resistor **1132** coupled in series between the first node N**1** and a voltage reference, for example ground. The timer capacitor **1131** and the timer resistor **1132** are coupled to each other at the fifth node N**5**. The timer capacitor **1131** can have a capacitance C**1** of about 0 pF to about 100 pF, for example, 2 pF. The timer resistor **1132** can have a resistance R**2** of about 0 MΩ to about 10 MΩ, for example, 2 MΩ.

[0134] The first voltage source **1130** includes a positive terminal coupled to the second node N**2** and a negative terminal coupled to the second voltage source **1140**. The second voltage source **1140** can have a positive terminal coupled to the negative terminal of the first voltage source **1130**, and a negative terminal coupled to a voltage reference, such as ground.

[0135] The base impedance block **1160** serves to provide the base impedance, similar to the base resistor **1060** of FIGS. **10**A and **10**B. The base impedance block **1160**, however, is turned on at a delayed time to provide impedance in response to the operation of the timer **1120**. The base impedance block **1160** can include one or more transistors **1161**-**1167** and a base resistor **1169**.

[0136] The transistors **1161**-**1167** are coupled in parallel to one another between the third node N**3** and the fourth node N**4**. In the illustrated embodiment, seven transistors are included in the base impedance block **1160**, but the number of transistors can vary widely, depending on the impedance to be provided by the base impedance block **1160**. Each of the transistors **1161**-**1167** can be an NMOS transistor having a source coupled to the fourth node N**4**, a drain coupled to the third node N**3**, and a gate coupled to the fifth node N**5**. In other embodiments, the base impedance block **1160** can be modified to include one or more PMOS transistors or NPN or PNP bipolar transistors in place of the NMOS transistors **1161**-**1167**. The base resistor **1169** has a first end coupled to the fourth node N**4** and a second end coupled to a voltage reference, for example, ground.

[0137] The emitter impedance block **1170** can include an emitter resistor. The emitter resistor can provide a resistance similar to that of the emitter resistor **1070** of FIGS. **10**A and **10**B. The emitter resistor **1170** can have a resistance R**1** of about 0Ω to about 200Ω, for example, 9Ω. In one embodiment, the emitter resistor can have the structure shown in FIG. **10**C.

[0138] During operation, when an ESD event occurs, the timer **1120** delays turning on the transistors **1161**-**1167** during a period of time substantially equal to the time constant τ of the timer **1120**. The time constant τ can be equal to R**2**×C**1**. During the period of time substantially equal to the time constant, the base impedance Zb is substantially greater than the emitter impedance Ze. Thus, the gain βn' of the device **1100** approaches the gain βn of the NPN transistor of the SCR **1110**.

[0139] After the period, the transistors **1161**-**1167** are turned on, thereby substantially reducing the base impedance Zb. Thus, the base impedance Zb is substantially smaller than the emitter impedance Ze. Thus, the gain βn' of the device **1100** approaches 0. Thus, the holding voltage of the device **1100** can be lowered by the operation of the timer **1120**.

[0140] FIG. **11**B shows a relationship between the TLP voltage and TLP current of the device **1100**. In FIG. **11**B, the trigger voltage is about 250 V, but the holding voltage is relatively lower, and is about 40 V.

[0141] Referring to FIG. **12**, an ESD protection device having a bipolar device configuration according to yet another embodiment will be described below. The illustrated protection device **1200** includes a bipolar transistor **1210**, a base resistor **1212**, a timer **1120**, a first voltage source **1130**, a second voltage source **1140**, a base impedance block **1160**, an emitter impedance block **1170**, and first to fifth nodes N**1**-N**5**.

[0142] The bipolar transistor **1210** can have a collector electrically coupled to the first voltage source **1130** via the second node N**2**, an emitter electrically coupled to the emitter impedance block **1170** via the first node N**1**, and a base electrically coupled to the base resistor **1212** via the third node N**3**. The collector and emitter of the bipolar transistor **1210** can be electrically coupled to first and second nodes, respectively, of an internal circuit to be protected. For example, the first and second nodes can be any two of the nodes **161**, **162**, **163**, **164** of FIG. **1**. The illustrated bipolar transistor **1210** is a non-symmetric device, and therefore its collector should be connected to the second node N**2**, and its emitter should be connected to the first node N**1**. Other details of the bipolar transistor **1210** can be as described above in connection with any one or more of FIGS. **4**A and **4**B, **5**A and **5**B, **5**C, **5**D, or **5**E.

[0143] The base resistor **1212** can have a first end coupled to the third node N**3**, and a second end coupled to a voltage reference, for example, ground. The base resistor **1212** can have a resistance R**3** of about 1 kΩ to about 30 kΩ, for example, 15 kΩ. The configurations of the timer **1120**, the first voltage source **1130**, the second voltage source **1140**, the